
		K S R INSTITUTE FOR ENGINEERING AND TECHNOLOGY (An Autonomous Institution) Approved by AICTE and Affiliated to Anna University, Chennai Accredited by NAAC ('A+' Grade) & NBA							Curriculum PG R - 2023		
Department		Department of Electrical and Electronics Engineering									
Programme		M.E. Embedded System Technologies									
SEMESTER I											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
Induction Programme			-	-	-	-	-	-	-	-	-
THEORY COURSES											
1	23MA1142	Applied Mathematics for Embedded Systems Technologists	FC	3	0	0	3	3	40	60	100
2	23RM1131	Research Methodology and IPR	RMC	3	0	0	3	3	40	60	100
3	23ET1101	Design of Embedded Systems	PCC	3	0	0	3	3	40	60	100
4	23ET1102	Software for Embedded Systems	PCC	3	0	0	3	3	40	60	100
5	23ET1103	Microcontroller Based System Design	PCC	3	0	0	3	3	40	60	100
6	23ET1104	VLSI Design and Reconfigurable Architecture	PCC	3	0	0	3	3	40	60	100
LABORATORY COURSES											
7	23ET1121	Embedded System Laboratory-I	PCC	0	0	4	4	2	60	40	100
8	23ET1122	Embedded Programming Laboratory - I	PCC	0	0	4	4	2	60	40	100
AUDIT COURSES											
9	23ET113#	Audit Course I*	AC	2	0	0	2	0	--	--	--
TOTAL				20	0	8	28	22	800		

*Audit course is optional

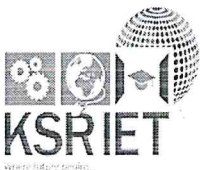

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	Department	Department of Electrical and Electronics Engineering	
Programme	M.E. Embedded System Technologies		

SEMESTER II											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
THEORY COURSES											
1	23ET1201	Real Time Operating System	PCC	3	0	0	3	3	40	60	100
2	23ET1202	Embedded System Networking	PCC	3	0	0	3	3	40	60	100
3	23ET1203	Embedded Control for Electric Drives	PCC	3	0	0	3	3	40	60	100
4	23ET1204	IoT for Smart Systems	PCC	3	0	0	3	3	40	60	100
5	23ET1P##	Professional Elective I	PEC	3	0	0	3	3	40	60	100
6	23ET1P##	Professional Elective II	PEC	3	0	0	3	3	40	60	100
LABORATORY COURSES											
7	23ET1221	Embedded System Laboratory - II	PCC	0	0	4	4	2	60	40	100
8	23ET1222	Embedded Programming Laboratory - II	PCC	0	0	4	4	2	60	40	100
AUDIT COURSES											
9	23ET113#	Audit Course II*	AC	2	0	0	2	0	--	--	--
TOTAL				20	0	8	28	22	800		


*Audit course is optional


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	K S R INSTITUTE FOR ENGINEERING AND TECHNOLOGY (An Autonomous Institution) Approved by AICTE and Affiliated to Anna University, Chennai Accredited by NAAC ('A+' Grade) & NBA		Curriculum PG R - 2023
	Department	Department of Electrical and Electronics Engineering	
	Programme	M.E. Embedded System Technologies	

SEMESTER III											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
THEORY COURSES											
1	23ET1P##	Professional Elective III	PEC	3	0	0	3	3	40	60	100
2	23ET1P##	Professional Elective IV	PEC	3	0	0	3	3	40	60	100
3	23ET1X##	Open Elective	OEC	3	0	0	3	3	40	60	100
EMPLOYABILITY ENHANCEMENT COURSES											
4	23ET1321	Project Work I	EEC	0	0	12	12	6	60	40	100
4	23ET1322	Technical Seminar	EEC	0	0	2	2	1	100	-	100
TOTAL				9	0	14	23	16	500		


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<p>Department</p>	<p align="center">Department of Electrical and Electronics Engineering</p>	
<p>Programme</p>	<p align="center">M.E. Embedded System Technologies</p>	

SEMESTER IV											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
EMPLOYABILITY ENHANCEMENT COURSES											
1	23ET1421	Project Work II	EEC	0	0	28	28	14	60	40	100
TOTAL				0	0	28	28	14	100		
TOTAL NO. OF CREDITS: 74											
TOTAL NUMBER OF CREDITS TO BE EARNED FOR AWARD OF THE DEGREE = 74											
Note: PCC-Professional Core Courses, PEC-Professional Elective Courses, OEC- Open Elective Courses, EEC- Employability Enhancement Courses & AC- Mandatory Courses, FC-Foundation Courses, RMC - Research Methodology and IPR Courses											



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FOUNDATION COURSES (FC)											
SEMESTER II											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
1.	23MA1142	Applied Mathematics for Embedded Systems Technologists	FC	3	0	0	3	3	40	60	100
TOTAL				3	0	0	3	3	40	60	100
PROFESSIONAL CORE COURSES (PCC)											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
1.	23ET1101	Design of Embedded Systems	PCC	3	0	0	3	3	40	60	100
2.	23ET1102	Software for Embedded Systems	PCC	3	0	0	3	3	40	60	100
3.	23ET1103	Microcontroller Based System Design	PCC	3	0	0	3	3	40	60	100
4.	23ET1104	VLSI Design and Reconfigurable Architecture	PCC	3	0	0	3	3	40	60	100
5.	23ET1121	Embedded System Laboratory - I	PCC	0	0	4	4	2	60	40	100
6.	23ET1122	Embedded Programming Laboratory -I	PCC	0	0	4	4	2	60	40	100
7.	23ET1201	Real Time Operating System	PCC	3	0	0	3	3	40	60	100
8.	23ET1202	Embedded System Networking	PCC	3	0	0	3	3	40	60	100
9.	23ET1203	Embedded Control for Electric Drives	PCC	3	0	0	3	3	40	60	100
10.	23ET1204	IoT for Smart Systems	PCC	3	0	0	3	3	40	60	100
11.	23ET1221	Embedded System Laboratory - II	PCC	0	0	4	4	2	60	40	100
12.	23ET1222	Embedded Programming Laboratory -II	PCC	0	0	4	4	2	60	40	100
TOTAL				24	0	16	40	32	1200		


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RESEARCH METHODOLOGY AND IPR COURSES (RMC)											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
1.	23RM1131	Research Methodology and IPR	RMC	3	0	0	3	3	40	60	100
TOTAL				3	0	0	3	3	100		
EMPLOYABILITY ENHANCEMENT COURSES (EEC)											
1.	23ET1321	Project Work I	EEC	0	0	12	12	6	60	40	100
2.	23ET1421	Project Work II	EEC	0	0	28	28	14	60	40	100
TOTAL				0	0	40	40	20	200		
PROFESSIONAL ELECTIVE SEMESTER II, ELECTIVE I & II											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
1.	23ET1P01	Wireless and Mobile Communication	PEC	3	0	0	3	3	40	60	100
2.	23ET1P 02	Virtual Instrumentation	PEC	3	0	0	3	3	40	60	100
3.	23ET1P 03	Embedded Processor Development	PEC	3	0	0	3	3	40	60	100
4.	23ET1P 04	Automotive Embedded System	PEC	3	0	0	3	3	40	60	100
5.	23ET1P 05	Intelligent Control and Automation	PEC	3	0	0	3	3	40	60	100
6.	23ET1P 06	Unmanned Aerial Vehicle	PEC	3	0	0	3	3	40	60	100
7.	23ET1P 07	DSP Based System Design	PEC	3	0	0	3	3	40	60	100
8.	23ET1P 08	Machine Learning and Deep Learning	PEC	3	0	0	3	3	40	60	100
TOTAL				24	0	0	24	24	800		


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SEMESTER III											
ELECTIVE III & IV											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
1.	23ET1P 09	Computer Vision	PEC	3	0	0	3	3	40	60	100
2.	23ET1P 10	Multimedia Communication	PEC	3	0	0	3	3	40	60	100
3.	23ET1P 11	Embedded Networking and Automation of Electrical System	PEC	3	0	0	3	3	40	60	100
4.	23ET1P 12	Smart System Design	PEC	3	0	0	3	3	40	60	100
5.	23ET1P 13	Embedded Computing	PEC	3	0	0	3	3	40	60	100
6.	23ET1P 14	Embedded Systems Security	PEC	3	0	0	3	3	40	60	100
7.	23ET1P 15	Robotics and Automation	PEC	3	0	0	3	3	40	60	100
8.	23ET1P 16	Reconfigurable Processor and SoC Design	PEC	3	0	0	3	3	40	60	100
9.	23ET1P 17	MEMS and NEMS Technology	PEC	3	0	0	3	3	40	60	100
10.	23ET1P 18	Entrepreneurship and Embedded Product Development	PEC	3	0	0	3	3	40	60	100
11.	23ET1P 19	Embedded System for Biomedical Applications	PEC	3	0	0	3	3	40	60	100
12.	23ET1P 20	Renewable Energy and Grid Integration	PEC	3	0	0	3	3	40	60	100
13.	23ET1P 21	Electric Vehicles and Power Management	PEC	3	0	0	3	3	40	60	100
14.	23ET1P 22	Python Programming for Machine Learning	PEC	3	0	0	3	3	40	60	100
15.	23ET1P 23	Smart Grid	PEC	3	0	0	3	3	40	60	100
TOTAL				45	0	0	45	45	1500		


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OPEN ELECTIVES FOR PG PROGRAMMES											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
1.	23CC1P01	Additive Manufacturing	OEC	3	0	0	3	3	40	60	100
2.	23CC1P02	New Product Development	OEC	3	0	0	3	3	40	60	100
3.	23CC1P03	Reverse Engineering	OEC	3	0	0	3	3	40	60	100
4.	23CC1P04	Industrial Safety Management	OEC	3	0	0	3	3	40	60	100
5.	23BD1X01	Big Data Security	OEC	3	0	0	3	3	40	60	100
6.	23BD1X02	Foundations Of Data Science	OEC	3	0	0	3	3	40	60	100
7.	23BD1X03	Web Analytics	OEC	3	0	0	3	3	40	60	100
8.	23BD1X04	Analytics Of Things	OEC	3	0	0	3	3	40	60	100
TOTAL				24	0	0	24	24	800		

AUDIT COURSES - I											
REGISTRATION FOR ANY OF THESE COURSES IS OPTIONAL TO STUDENTS											
S. No.	Course Code	Course Title	Category	Periods / Week				Credit	Max. Marks		
				L	T	P	Tot		CA	ES	Tot
1.	23ET1131	English for Research Paper Writing	AC	2	0	0	2	0	--	--	--
2.	23ET1132	Disaster Management	AC	2	0	0	2	0	--	--	--
3.	23ET1133	Constitution of India	AC	2	0	0	2	0	--	--	--
4.	23ET1134	நற்றமிழ் இலக்கியம்	AC	2	0	0	2	0	--	--	--
TOTAL				8	0	0	8	0	---		

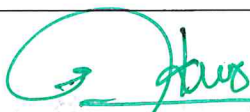

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 (2023)

SUMMARY

S.No	Name of the Programme: M.E.EMBEDDED SYSTEMS TECHNOLOGIES					
	SUBJECT AREA	CREDITS PER SEMESTER				CREDITS TOTAL
I		II	III	IV		
1	FC	3				3
2	PCC	16	16			32
3	PEC		6	6		12
4	RMC	3				3
5	OEC			3		3
6	EEC			7	14	21
7	Non Credit/Audit Course					-
8	TOTAL CREDIT	22	22	16	14	74


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23MA1142	APPLIED MATHEMATICS FOR EMBEDDED SYSTEMS TECHNOLOGISTS	Category	L	T	P	C
		FC	3	0	0	3
OBJECTIVES: The Course will enable learners to: <ul style="list-style-type: none"> ❖ To understand the techniques of Fourier transform to solve partial differential equations. ❖ To become familiar with graph theory for modelling the embedded system. ❖ To understand various optimization techniques for utilizing system and network resources. ❖ To understand the basic concepts of probability to apply in embedded technology. ❖ To understand the basic concept of random variables and queuing theories to address stochastic and dynamic environment in embedded technology. 						
UNIT - I	FOURIER TRANSFORM TECHNIQUES FOR PARTIAL DIFFERENTIAL EQUATIONS	9				
Fourier transform: Definitions - Properties – Transform of elementary functions - Dirac delta function – Convolution theorem – Parseval's identity – Solutions to partial differential equations : Heat equation Wave equation - Laplace and Poisson's equations.						
UNIT - II	GRAPH THEORY	9				
Introduction to paths, trees, vector spaces - Matrix coloring and directed graphs - Some basic algorithms – Shortest path algorithms – Depth - First search on a graph – Isomorphism – Other Graph -Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.						
UNIT - III	OPTIMIZATION TECHNIQUES	9				
Linear programming - Basic concepts – Graphical and simplex methods – Big M method - Two phase simplex method - Revised simplex method - Transportation problems – Assignment problems .						
UNIT – IV	PROBABILITY AND RANDOM VARIABLES	9				
Probability – Axioms of probability – Conditional probability – Baye's theorem - Random variables - Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Exponential, Normal distributions – Two dimensional random variables - Poisson process.						
UNIT - V	QUEUEING THEORY	9				
Single and multiple servers - Markovian queuing models - Finite and infinite capacity queues – Finitesource model – Queuing applications.						
TOTAL: 45 PERIODS						


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COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Apply Fourier transform techniques to solve PDE technology.	Apply
CO2	Model the networks in embedded systems using graph theory.	Apply
CO3	Use the ideas of probability and random variables in solving engineering problems.	Apply
CO4	Use the ideas of random variables in solving engineering problems.	Apply
CO5	Address stochastic and dynamic behavior of data transfer using queuing theories in embedded systems technologies.	Apply

TEXT BOOKS:

1	Taha H .A., " Operations Research: An Introduction " , 9 th Edition, Pearson Education Asia, New Delhi, 2016.
2	Walpole R.E., Myer R.H., Myer S.L., and Ye, K., " Probability and Statistics for Engineers and Scientists ", 7 th Edition, Pearson Education, Delhi, 2002

REFERENCES:

1	Sankara Rao, K., " Introduction to Partial Differential Equations ", Prentice Hall of India Pvt. Ltd., New Delhi, 1997.
2	Narasingh Deo, " Graph Theory with Applications to Engineering and Computer Science ", Prentice Hall India, 1997.
3	S. S. Rao, " Engineering Optimization, Theory and Practice ", 4 th Edition, John Wiley and Sons, 2009.

Mapping of COs with POs and PSOs

COs / POs	PO 1	PO2	PO 3	PO4	PO 5	PO6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO2
CO1	3	2	2	1	3	2	-	-	-	1	-	3	-	2
CO2	3	2	2	2	3	2	-	-	-	1	-	3	-	2
CO3	3	2	2	2	3	3	-	-	-	1	-	3	-	2
CO4	3	2	2	1	3	3	-	-	-	1	-	3	-	2
CO5	3	2	2	3	3	3	-	-	-	1	-	3	-	2
Avg.	3	2	2	1.8	3	2.6	-	-	-	1	-	3	-	2


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ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


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23RM1131	RESEARCH METHODOLOGY AND IPR	Category	L	T	P	C
		RM	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> ❖ To understand the techniques of Fourier transform to solve partial differential equations. ❖ To become familiar with graph theory for modelling the embedded system. ❖ To understand various optimization techniques for utilizing system and network resources. ❖ To understand the basic concepts of probability to apply in embedded technology. ❖ To understand the basic concept of random variables and queuing theories to address stochastic and dynamic environment in embedded technology. 						
UNIT - I	RESEARCH DESIGN					9
Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys						
UNIT - II	DATA COLLECTION AND SOURCES					9
Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.						
UNIT - III	DATA ANALYSIS AND REPORTING					9
Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation. UNIT IV						
UNIT - IV	INTELLECTUAL PROPERTY RIGHTS					9
Intellectual Property — The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance						
UNIT - V	PATENTS					9
Patents — objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filing, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.						
TOTAL: 45 PERIODS						


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COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Design a suitable research process to solve business problem.	Apply
CO2	Describe and apply appropriate methods to collect qualitative and quantitative data for analysis.	Apply
CO3	Describe and apply appropriate statistical tools to analyze data and solve research problems.	Apply
CO4	Describe about the types and features of intellectual property and its role for IPR establishment.	Apply
CO5	Illustrate the patent procedures, E-filing, register of patents and licensing of patents.	Apply

TEXT BOOKS:

1	Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education, 11e (2012).
2	Catherine J. Holland, "Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets", Entrepreneur Press, 2007.

REFERENCES:

1	David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
2	The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.

Mapping of COs with POs and PSOs

COs/ POs	PO 1	P O2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO2
CO1	2	1	2	2	--	1	1	2	--	1	--	1	--	2
CO2	2	1	2	--	--	1	1	2	--	1	--	1	--	2
CO3	2	1	2	2	2	1	1	2	--	1	--	1	--	2
CO4	2	1	2	--	--	1	1	2	--	1	--	1	--	2
CO5	2	1	2	--	--	1	1	2	--	1	--	1	--	2
Avg.	2	1	2	2	2	1	1	2	--	1	--	1	--	2


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ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


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23ET1101	DESIGN OF EMBEDDED SYSTEMS	Category	L	T	P	C
		PCC	3	0	0	3
OBJECTIVES:						
<p>The Course will enable learners to:</p> <ul style="list-style-type: none"> ❖ To provide knowledge on the basics, building blocks of Embedded System. ❖ To discuss Input/output Interfacing & Bus Communication with processors. ❖ To teach automation using scheduling algorithms and Real time operating system. ❖ To discuss on different Phases & Modeling of a new embedded product. ❖ To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employability skills 						
UNIT - I	INTRODUCTION TO EMBEDDED SYSTEMS	9				
Introduction to Embedded Systems –built in features for embedded Target Architecture - selection of Embedded processor – DMA- memory devices – Memory management methods-memory mapping, cache replacement policies- Timer and Counting devices, Watchdog Timer, Real Time Clock- Software Development tools-IDE, assembler, compiler, linker, simulator, debugger, In circuit emulator, Target Hardware Debugging- Overview of functional safety standards for embedded systems.						
UNIT - II	EMBEDDED NETWORKING BY PROCESSORS	9				
Embedded Networking: Introduction, I/O Device Ports & Buses- multiple interrupts and interrupt service mechanism – Serial Bus communication protocols -RS232 standard–RS485–USB–Inter Integrated Circuits (I ² C)- CAN Bus –Wireless protocol based on Wifi , Bluetooth, Zigbee – Introduction to Device Drivers						
UNIT - III	RTOS BASED EMBEDDED SYSTEM DESIGN	9				
Introduction to basic concepts of RTOS- Need, Task, process & threads, interrupt routines in RTOS, Multiprocessing and Multitasking, Preemptive and non-preemptive scheduling, Task communication- context switching, interrupt latency and deadline shared memory, message passing- , Interprocess Communication – synchronization between processes-semaphores, Mailbox, pipes, priority inversion, priority inheritance, comparison of Real time Operating systems: VxWorks, uC/OS-II, RT Linux.						
UNIT – IV	MODELLING WITH HARDWARE/SOFTWARE DESIGN APPROACHES	9				
Modelling embedded systems- embedded software development approach --Overview of UML modeling with UML, UML Diagrams-- Hardware/Software Partitioning , Co-Design Approaches for System Specification and modeling- CoSynthesis- features comparing Single-processor Architectures & Multi-Processor Architectures--design approach on parallelism in uniprocessors & Multiprocessors.						
UNIT - V	EMBEDDED SYSTEM APPLICATION DEVELOPMENT	9				
Objective, Need, different Phases & Modelling of the EDLC. choice of Target Architectures for Embedded Application Development-for Control Dominated-Data Dominated Systems- Case studies on Digital Camera, Adaptive Cruise control in a Car, Mobile Phone software for key inputs.						
TOTAL: 45 PERIODS						


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COURSE OUTCOMES:		
Upon completion of the course, the students will be able to:		
Course Outcome	Description	Bloom's Taxonomy Level
CO1	Demonstrate the functionalities of processor internal blocks, with their requirement.	Understand
CO2	Analyze that Bus standards are chosen based on interface overheads without sacrificing processor performance	Analyze
CO3	Explain the role and features of RT operating system, that makes multitask execution possible by processors.	Apply
CO4	Illustrate that using multiple CPU based on either hardcore or softcore helps data overhead management with processing- speed reduction for uC execution	Apply
CO5	Recommend Embedded consumer product design based on phases of product development.	Apply
TEXT BOOKS:		
1	Rajkamal, 'Embedded system-Architecture, Programming, Design', TMH,2011.	
2	Peckol, "Embedded system Design", John Wiley & Sons, 2010	
3	Lyla B Das, "Embedded Systems-An Integrated Approach", Pearson 2013	
REFERENCES:		
1	Advanced Computer architecture , By Rajiv Chopra, S Chand , 2010	
2	Elicia White, "Making Embedded Systems", O'Reilly Series, SPD, 2011	
3	Bruce Powel Douglass, "Real-Time UML Workshop for Embedded Systems, Elsevier, 2011	

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	3	2	1	-	-	-	-	1	-	3	-	2
CO2	2	-	1	2	-	-	-	-	-	1	-	3	-	2
CO3	-	2	2	3	-	-	-	-	-	1	-	3	-	2
CO4	2	-	3	3	-	-	-	-	-	1	-	3	-	2
CO5	2	-	1	2	-	2	-	-	-	1	-	3	-	2
Avg.	2	2	2	2.4	1	2	-	-	-	1	-	3	-	2


 Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


 Chairman (BoS)

23ET1102	SOFTWARE FOR EMBEDDED SYSTEMS	Category	L	T	P	C
		PCC	3	0	0	3
OBJECTIVES:						
<p>The Course will enable learners to:</p> <ul style="list-style-type: none"> ❖ To expose the students to the fundamentals of embedded Programming ❖ To Introduce the GNU C Programming Tool Chain in Linux. ❖ To study the basic concepts of embedded C. ❖ To teach the basics of Python Programming ❖ To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts 						
UNIT - I	BASIC C PROGRAMMING	9				
Typical C Program Development Environment - Introduction to C Programming - Structured Program Development in C - Data Types and Operators - C Program Control - C Functions - Introduction to Arrays.						
UNIT - II	EMBEDDED C	9				
Adding Structure to 'C' Code: Object oriented programming with C, Header files for Project and Port, Examples. Meeting Real-time constraints: Creating hardware delays - Need for timeout mechanism - Creating loop timeouts - Creating hardware timeouts.						
UNIT - III	C PROGRAMMING TOOL-CHAIN IN LINUX	9				
C preprocessor - Stages of Compilation - Introduction to GCC - Debugging with GDB - The Make utility - GNU Configure and Build System - GNU Binary utilities - Profiling - using gprof - Introduction to GNU C Library						
UNIT - IV	PYTHON PROGRAMMING	9				
Introduction - Parts of Python Programming Language - Control Flow Statements - Functions - Strings Lists - Dictionaries - Tuples and Sets						
UNIT - V	MODULES, PACKAGES AND LIBRARIES IN PYTHON	9				
Python Modules and Packages - Creating Modules and Packages - Practical Example - Libraries for Python - Library for Mathematical functionalities and Tools - Numerical Plotting Library - GUI Libraries for Python - Imaging Libraries for Python - Networking Libraries						
TOTAL: 45 PERIODS						


 Chairman (BoS)

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Demonstrate C programming and its salient features for embedded systems	Understand
CO2	Deliver insight into various programming languages/software compatible to embedded process development with improved design & programming skills.	Analyze
CO3	Develop knowledge on C programming in Linux environment..	Apply
CO4	Possess ability to write python programming for Embedded applications.	Apply
CO5	Have improved Employability and entrepreneurship capacity due to knowledge upgradation on recent trends in embedded programming skills	Apply

TEXT BOOKS:

1	Paul Deitel and Harvey Deitel, "C How to Program", 8th Edition, Pearson Education Limited, 2016.
2	Michael J Pont, "Embedded C", Addison-Wesley, An imprint of Pearson Education, 2002.
3	William von Hagen, "The Definitive Guide to GCC", 2nd Edition, Apress Inc., 2006

REFERENCES:

1	Gowrishankar S and Veena A, "Introduction to Python Programming", CRC Press, Taylor & Francis Group, 2019
2	Noel Kalicharan, "Learn to Program with C", Apress Inc., 2015.
3	Steve Oualline, "Practical C programming", O'Reilly Media, 1997.

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	2	-	3	-	-	-	-	1	-	3	-	2
CO2	1	-	1	-	2	-	-	-	-	1	-	3	-	2
CO3	-	2	-	-	2	-	-	-	-	1	-	3	-	2
CO4	1	-	1	1	1	-	-	-	-	1	-	3	-	2
CO5	-	-	2	2	3	2	-	-	-	1	-	3	-	2
Avg.	1	2	1.5	1,5	2.2	2	-	-	-	1	-	3	-	2


 Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1103	MICROCONTROLLER BASED SYSTEM DESIGN	Category	L	T	P	C
		PCC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> To teach the architecture of PIC Microcontroller and RISC processor. To compare the architecture and programming of 8,16,32 bit RISC processor To teach the implementation of DSP in ARM processor. To discuss on memory management, application development in RISC processor To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquired over the 5 Units of the subject for improved employability skills. 						
UNIT - I	PIC MICROCONTROLLER					6
Architecture – memory organization – addressing modes – instruction set – PIC programming in Assembly & C –I/O port, Data Conversion, RAM & ROM Allocation, Timer programming, practice inMP-LAB						
UNIT - II	ARM ARCHITECTURE					9
Architecture – memory organization – addressing modes –The ARM Programmer’s model - Registers– Pipeline - Interrupts – Coprocessors – Interrupt Structure						
UNIT - III	PERIPHERALS OF PIC AND ARM MICROCONTROLLER					9
PIC: ADC, DAC and Sensor Interfacing –Flash and EEPROM memories. ARM: I/O Memory – EEPROM – I/O Ports – SRAM –Timer –UART - Serial Communication with PC – ADC/DAC Interfacing.						
UNIT – IV	ARM MICROCONTROLLER PROGRAMMING					9
ARM general Instruction set – Thumb instruction set –Introduction to DSP on ARM – Implementationexample of Filters						
UNIT - V	DESIGN WITH PIC AND ARM MICROCONTROLLERS					9
PIC implementation - Generation of Gate signals for converters and Inverters - Motor Control – Controlling DC/ AC appliances – Measurement of frequency - Stand aloneData Acquisition System –ARM Implementation- Simple ASM/C programs- Loops –Look up table- Block copy- subroutines-Hamming Code						
TOTAL: 45 PERIODS						


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Chairman (BoS)

COURSE OUTCOMES:		
Upon completion of the course, the students will be able to:		
Course Outcome	Description	Bloom's Taxonomy Level
CO1	Understand the basics and requirement of processor functional blocks	Understand
CO2	Observe the specialty of RISC processor Architecture	Apply
CO3	Incorporate I/O hardware interface of a processor based automation for consumer application with peripherals	Apply
CO4	Incorporate I/O software interface of a processor with peripherals.	Apply
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in commercial embedded processors	Apply
TEXT BOOKS:		
1	Steve Furber, 'ARM system on chip architecture', Addison Wesley, 2010.	
2	Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield 'ARM System Developer's Guide Designing and Optimizing System Software', Elsevier 2007.	
REFERENCES:		
1	Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey 'PIC Microcontroller and Embedded Systems using Assembly and C for PIC18', Pearson Education 2008.	
2	John Iovine, 'PIC Microcontroller Project Book ', McGraw Hill 2000	
3	ARM Architecture Reference Manual, LPC213x User Manual	

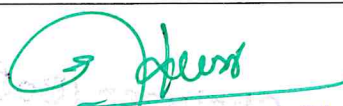
Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	2	-	-	-	-	-	-	1	-	3	-	2
CO2	1	-	3	2	-	-	-	-	-	1	-	3	-	2
CO3	-	-	1	3	1	-	-	-	-	1	-	3	-	2
CO4	1	-	-	1	2	-	-	-	-	1	-	3	-	2
CO5	-	-	2	-	-	-	-	-	-	1	-	3	-	2
Avg.	1	-	2	2	1.5	-	-	-	-	1	-	3	-	2


 Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1104	VLSI DESIGN AND RECONFIGURABLE ARCHITECTURE	Category	L	T	P	C
		PCC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> To expose the students to the fundamentals of sequential system design, synchronous and Asynchronous circuits. To understand the basic concepts of CMOS and to introduce the IC fabrication methods To introduce the Reconfigurable Processor technologies, To provide an insight and architecture significance of SOC. To introduce the basics of analog VLSI design and its importance. To learn about the programming of Programmable device using Hardware description Language. 						
UNIT - I	INTRODUCTION TO ADVANCED DIGITAL SYSTEM DESIGN	9				
Modeling of Clocked Synchronous Sequential Network(CSSN), Design of CSSN, Design of Asynchronous Sequential Circuits (ASC), Designing Vending Machine Controller, Races in ASC, Static and Dynamic Hazards, Essential Hazards, Designing Hazard free circuits.						
UNIT - II	CMOS BASICS & IC FABRICATION	9				
Moore's Law-MOSFET Scaling - MOS Transistor Model-Determination of pull up / pull down ratios- CMOS based combinational logic & sequential design- Dynamic CMOS –Transmission Gates- BiCMOS- Low power VLSI – CMOS IC Fabrications - Stick Diagrams, Design Rules and Layout.						
UNIT - III	ASIC AND RECONFIGURABLE PROCESSOR AND SoC DESIGN	9				
Introduction to ASIC, ASIC design flow- programmable ASICs- Introduction to reconfigurable processor- Architecture -Reconfigurable Computing, SoC Overview, recent trends in Reconfigurable Processor & SoC, Reconfigurable processor based DC motor control						
UNIT – IV	ANALOG VLSI DESIGN	9				
Introduction to analog VLSI- Design of CMOS 2stage-3 stage Op-Amp –High Speed and High frequency op-amps-Super MOS- Analog primitive cells- Introduction to FPAA						
UNIT - V	HDL PROGRAMMING	9				
Overview of digital design with VHDL, structural, data flow and behavioural modeling concepts- logic synthesis-simulation-Design examples, Ripple carry Adders, Carry Look ahead adders, Multiplier, ALU, Shift Registers, Test Bench.						
TOTAL: 45 PERIODS						


 Chairman (BoS)

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Incorporate synchronous and asynchronous switching logics, with clocked circuits design	Apply
CO2	Deliver insight into developing CMOS design techniques and IC fabrication methods.	Apply
CO3	Explain the need of reconfigurable computing, hardware-software co design and operation of SoC processor.	Analyze
CO4	Design and development of reprogrammable analog devices and its usage for Embedded applications.	Analyze
CO5	Illustrate and develop HDL computational processes with improved design strategies.	Apply

TEXT BOOKS:

- 1 Donald G. Givone, "Digital principles and Design", Tata McGraw Hill 2002.
- 2 Charles H. Roth Jr., "Fundamentals of Logic design", Thomson Learning, 2004.

REFERENCES:

- 1 Nurmi, Jari (Ed.) "Processor Design System-On-Chip Computing for ASICs and FPGAs" Springer, 2007.
- 2 Joao Cardoso, Michael Hübner, "Reconfigurable Computing: From FPGAs to Hardware/Software Codesign" Springer, 2011.
- 3 Pierre-Emmanuel Gaillardon, Reconfigurable Logic: Architecture, Tools, and Applications, 1st Edition, CRC Press, 2015

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	1	-	-	-	-	-	1	-	3	-	2
CO2	2	-	2	2	-	-	-	-	-	1	-	3	-	2
CO3	-	-	3	3	2	1	-	-	-	1	-	3	-	2
CO4	2	-	2	3	1	-	-	-	-	1	-	3	-	2
CO5	-	1	1	3	3	1	-	-	-	1	-	3	-	2
Avg.	2	1	2	2.4	2	1	-	-	-	1	-	3	-	2


Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


 Chairman (BoS)

23ET1121	EMBEDDED SYSTEM LABORATORY-I	Category	L	T	P	C
		PCC	0	0	4	2
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> • To involve the students to Practice on Workbench /Software Tools/ Hardware ProcessorBoards with the supporting Peripherals. • To teach the concepts of algorithm development & programming on software tools andDigital processors with peripheral interfaces. • To encourage students to practice in open-source software / packages /tools • To train though hands-on practices in commercial and licensed Hardware-software suites • Practicing through the subdivisions covered within experiments listed below to exposethe students into the revising the concepts acquired from theory subjects 						
LIST OF EXPERIMENTS						45
<ul style="list-style-type: none"> ▪ Programming with 8 bit Microcontrollers# Assembly programming ▪ Programming with 8 bit Microcontrollers# C programming ▪ I/O Programming with 8 bitMicrocontrollers ▪ I/O Interfacing : Serial port programming/ LCD/Sensor Interfacing /PWM Generation/ Motor Control ▪ Programming with PIC Microcontrollers <ul style="list-style-type: none"> - Assembly - C programming ▪ I/O Programming with PICMicrocontrollers I/O Interfacing: PWM Generation/ MotorControl/ADC/DAC/ LCD/Sensor Interfacing 						
EQUIPMENT/ SUPPORTS REQUIRED						
<ul style="list-style-type: none"> • 8051/ other8 bit Microcontrollers withperipherals; IDE, Board Support Software Tools / Compiler/others • 8051 Microcontrollers with peripherals; IDE, Board Support Software Tools /CCompiler/others • 8051 Microcontrollers with peripherals; Board Support Software Tools, peripherals withinterface • PIC Microcontrollers with peripherals; ;IDE, Board Support Software Tools /C Compiler/others • PIC Microcontrollers with peripherals; Board Support Software Tools, peripherals with interface 						
TOTAL: 45 PERIODS						

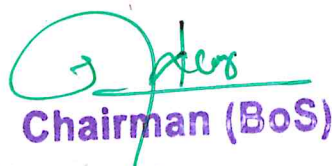


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COURSE OUTCOMES:		
Upon completion of the course, the students will be able to:		
Course Outcome	Description	Bloom's Taxonomy Level
CO1	Experiment insight into various embedded processors of CISC and RISC architecture /computational processors with peripheral interface.	Apply
CO2	Understand the fundamental concepts of how process can be controlled with uC.	Apply
CO3	Experimenting on programming logic of Processor based on software suites(simulators,emulators)	Apply
CO4	Incorporate I/O software interface of a processor with peripherals.	Apply
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in interfacing and use of commercial embedded processors	Apply
TEXT BOOKS:		
1	Mohammad Ali Mazidi&Mazidi ' 8051 Microcontroller and Embedded Systems', Pearson Education	
2	Simon Monk," Make Action-with Arduino and Raspberry Pi,SPD ,2016	
REFERENCES:		
1	Taan S.Elali,"Discrete Systems and Digital Signal Processing with Matlab",CRC Press2009.	
2	JovithaJerome,"Virtual Instrumentation using Labview"PHI,2010.	
3	Woon-Seng Gan, Sen M. Kuo, 'Embedded Signal Processing with the Micro Signal Architecture', John Wiley & Sons, Inc., Hoboken, New Jersey 2007	

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	2	1	-	-	-	-	-	1	-	3	-	2
CO2	-	-	1	1	2	1	-	-	-	1	-	3	-	2
CO3	2	3	1	2	3	-	-	-	-	1	-	3	-	2
CO4	2	-	2	1	2	-	-	-	-	1	-	3	-	2
CO5	-	-	1	1	3	2	-	-	-	1	-	3	-	2
Avg.	2	2	1.4	1.2	2.5	1.5	-	-	-	1	-	3	-	2

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Chairman (BoS)

ASSESSMENT SYSTEM:						
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)	
0	0	4	2	Laboratory only (60%)	Laboratory only (40%)	
LABORATORY						
Evaluation Laboratory Record				Model Practical		Max CIE Marks
75*				25*		100*
Total Marks shall be converted in to 60						


Chairman (BoS)

23ET1122	EMBEDDED PROGRAMMING LABORATORY – I	Category	L	T	P	C
		PCC	0	0	4	2
<p>OBJECTIVES:</p> <p>The Course will enable learners to:</p> <ul style="list-style-type: none"> To involve the students to Practice on Workbench /Software Tools/ Hardware ProcessorBoards with the supporting Peripherals. To teach the concepts of algorithm development & programming on software tools andDigital processors with peripheral interfaces. To encourage students to practice in open source softwares / packages /tools To train though hands-on practices in commercial and licensed Hardware-software suites Practicing through the subdivisions covered within experiments listed below to expose the students into the revising the concepts acquired from theory subjects. 						
LIST OF EXPERIMENTS					45	
<ul style="list-style-type: none"> Programming in HigherLevel Languages/OpenSource Platforms Programming with ArduinoMicrocontroller Board HDL Programming in FPGAprocessors Programming & Simulationin Simulators /Tools/others Programming & Simulationin Simulators /Tools/others <p>EQUIPMENT/ SUPPORTS REQUIRED</p> <ul style="list-style-type: none"> C/C++/Java/Embedded C/Embedded Java/Compilers &Platforms/cloud Arduino Boards with peripherals ;IDE,Board Support SoftwareTools/Compiler/others Processor Boards with Board SupportTools & Interfaces Simulation Tools as Proteus/ ORCAD Simulation Tools as MATLAB /others 						
TOTAL: 45 PERIODS						

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Developing Optimized code for embedded processor	Apply
CO2	Understanding the fundamental concepts of how process can be realized using Software Modules	Apply
CO3	Circuit and System level simulators to develop solution for embedded based applications	Apply
CO4	Incorporate I/O software interface of a processor with peripherals.	Apply
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on Embedded computing and algorithm development with programming concepts	Apply

TEXT BOOKS:

1	Mohammad Ali Mazidi & Mazidi ' 8051 Microcontroller and Embedded Systems', Pearson Education
2	Simon Monk, " Make Action-with Arduino and Raspberry Pi, SPD ,2016

REFERENCES:

1	Taan S.Elali, "Discrete Systems and Digital Signal Processing with Matlab", CRC Press 2009.
2	Jovitha Jerome, "Virtual Instrumentation using Labview" PHI, 2010.
3	Woon-Seng Gan, Sen M. Kuo, 'Embedded Signal Processing with the Micro Signal Architecture', John Wiley & Sons, Inc., Hoboken, New Jersey 2007

Mapping of COs with POs and PSOs

COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	1	2	2	1	-	-	-	1	-	3	-	2
CO2	2	-	2	-	3	2	-	-	-	1	-	3	-	2
CO3	2	1	3	1	2	2	-	-	-	1	-	3	-	2
CO4	2	1	2	2	2	-	-	-	-	1	-	3	-	2
CO5	-	-	2	-	3	1	-	-	-	1	-	3	-	2
Avg.	2	1	2	1.6	2.4	1.5	-	-	-	1	-	3	-	2

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Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
0	0	4	2	Laboratory only (60%)	Laboratory only (40%)
LABORATORY					
Evaluation Laboratory Record			Model Practical		Max CIE Marks
75*			25*		100*
Total Marks shall be converted in to 60					


Chairman (BoS)

23ET1201	REAL TIME OPERATING SYSTEM	Category	L	T	P	C
		PCC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ol style="list-style-type: none"> 1. To expose the students to the fundamentals of interaction of OS with a computer and Usercomputation. 2. To teach the fundamental concepts of how process are created and controlled with OS. 3. To study on programming logic of modeling Process based on range of OS features 4. To compare types and Functionalities in commercial OS, application development using RTOS 5. To involve Discussions/ Practice/Exercise onto revising & familiarizing the concepts acquiredover the 5 Units of the subject for improved employability skills 						
UNIT - I	REVIEW OF OPERATING SYSTEMS	9				
Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes – Introduction to Distributed operating system – Embedded operating systems						
UNIT - II	OVERVIEW OF RTOS	9				
RTOS Task and Task state –Multithreaded Preemptive scheduler- Process Synchronization- Message queues– Mail boxes -pipes – Critical section – Semaphores – Classical synchronization problem – Deadlocks						
UNIT - III	REALTIME MODELS AND LANGUAGES	9				
Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RTscheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.						
UNIT – IV	REALTIME KERNEL	9				
Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and Basic study of various RTOS like – VX works – Linux supportive RTOS – C Executive.						
UNIT - V	APPLICATION DEVELOPMENT	9				
Discussions on Basics of Linux supportive RTOS – uCOS-C Executive for development of RTOS Application – Case study						
TOTAL: 45 PERIODS						


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COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Understand Operating System structures and types	Understand
CO2	Insight into scheduling, disciplining of various processes execution	Apply
CO3	Illustrate knowledge on various RTOS support modelling	Analyze
CO4	Demonstrate commercial RTOS Suite features to work on real time processes design	Analyze
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in RTOS and embedded automation design.	Apply

TEXT BOOKS:

- 1 Silberschatz, Galvin, Gagne" Operating System Concepts, 6th ed, John Wiley, 2003
- 2 Charles Crowley, "Operating Systems-A Design Oriented approach" McGraw Hill, 1997

REFERENCES:

- 1 Raj Kamal, "Embedded Systems- Architecture, Programming and Design" Tata McGrawHill, 2006.
- 2 Karim Yaghmour, "Building Embedded Linux System", O'reilly Pub, 2003
- 3 Mukesh Sigal and N G Shi "Advanced Concepts in Operating System", McGraw Hill, 2000

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	1	-	2	-	-	-	-	1	-	3	-	2
CO2	-	-	2	-	3	1	-	-	-	1	-	3	-	2
CO3	2	-	2	1	2	2	-	-	-	1	-	3	-	2
CO4	2	2	3	2	1	3	-	-	-	1	-	3	-	2
CO5	-	-	1	-	3	1	-	-	-	1	-	3	-	2
Avg.	2	2	1.8	1.5	2.2	1.75	-	-	-	1	-	3	-	2


Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1202	EMBEDDED SYSTEM NETWORKING	Category	L	T	P	C
		PCC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> To expose the students to the fundamentals of wired embedded networking techniques. To introduce the concepts of embedded ethernet. To expose the students to the fundamentals of wireless embedded networking. To discuss the fundamental building blocks of digital instrumentation. To introduce design of Programmable measurement & control of electrical Device. 						
UNIT - I	EMBEDDED PROCESS COMMUNICATION WITH INSTRUMENT BUS	9				
Embedded networking: Introduction – Cluster of instruments in System: Introduction to bus protocols – comparison of bus protocols – RS 232C, RS 422, RS 485 and USB standards – embedded ethernet –MOD bus, LIN bus and CAN bus						
UNIT - II	EMBEDDED ETHERNET	9				
Elements of a network – Inside Ethernet – Building a Network : Hardware options – Cables, Connections and network speed – Ethernet controllers – Inside the internet protocol – Exchanging messages using UDP and TCP – Email for Embedded systems using FTP – Keeping devices and network secure						
UNIT - III	WIRELESS EMBEDDED NETWORKING	9				
Wireless sensor networks – Introduction – Node architecture – Network topology - Localization – Timesynchronization – Energy efficient MAC protocols – SMAC – Energy efficient and robust routing – Data centric routing - WSN Applications - Home Control - Building Automation - Industrial Automation						
UNIT – IV	BUILDING SYSTEM AUTOMATION	9				
Sensor Types & Characteristics: Sensing Voltage, Current, flux, Torque, Position, Proximity, Accelerometer - Data acquisition system- Signal conditioning circuit design- Uc Based & PC based data acquisition – UC for automation and protection of electrical appliances –processor based digital controllers for switching Actuators: Stepper motors, Relays –System automation with multi-channel Instrumentation and interface						
UNIT - V	COMMUNICATION FOR LARGE ELECTRICAL SYSTEM AUTOMATION	9				
Data Acquisition, Monitoring, Communication, Event Processing, and Polling Principles, SCADA system principles – outage management– Decision support application - substation automation, extended control feeder automation, Performance measure and response time, SCADA Data Models, need, sources, interface						
TOTAL: 45 PERIODS						


 (BoS) Chairman (BoS)

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Analyze the different bus communication protocols used for embedded networking	Analyze
CO2	Explain the basic concepts of embedded networking	Understand
CO3	Apply the embedded networking concepts in wireless networks	Apply
CO4	Relate different data acquisition concepts	Apply
CO5	Build a system automation for different applications	Apply

TEXT BOOKS:

1	Mohammad Ilyas And ImadMahgoub, 'Handbook of sensor Networks: Compact wireless andwired sensing systems', CRC Press,2005
2	Peter W Gofton , "Understanding Serial Communication", Sybes International, 2000

REFERENCES:

1	Jan Axelson 'Embedded Ethernet and Internet Complete', Penram publications
2	Krzysztof Iniewski,"Smart Grid ,Infrastructure& Networking",TMcGH,2012
3	Control and automation of electrical power distribution systems, James Northcote-Green,Robert Wilson, CRC, Taylor and Francis, 2006


Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	2	-	-	3	1	-	-	-	1	-	3	-	2
CO2	-	2	-	-	2	1	-	-	-	1	-	3	-	2
CO3	3	2	2	3	2	3	-	-	-	1	-	3	-	2
CO4	2	-	3	3	-	2	-	-	-	1	-	3	-	2
CO5	3	-	3	3	-	2	-	-	-	1	-	3	-	2
Avg.	2.25	2	2.7	3	2.3	1.8	-	-	-	1	-	3	-	2


Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1203	EMBEDDED CONTROL FOR ELECTRIC DRIVES	Category	L	T	P	C
		PCC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> • To provide the control concept for electrical drives • To emphasis the need for embedded system for controlling the electrical drives • To provide knowledge about various embedded system based control strategy for electric drives • To Impart the knowledge of optimization and machine learning techniques used for electrical drives • To familiarize the high performance computing for electrical drives. 						
UNIT - I	INTRODUCTION ELECTRICAL DRIVES	9				
Electric drive and its classifications, Four-quadrant drive, Dependence of load torque on various factors, Dynamics of motor-load combination-Solid State Controlled Drives-Machine learning and optimization techniques for electrical drives- IoT for Electrical drives applications.						
UNIT - II	OVERVIEW OF EMBEDDED PROCESSOR	9				
Embedded Processor architecture-RTOS – Hardware/software co-design-Programming with SoC processors						
UNIT - III	INDUCTION MOTOR CONTROL	9				
Types- Speed control methods-PWM techniques- VSI fed three-phase induction motor- Fuzzy logic Based speed control for three phase induction motor-FPGA based three phase induction motor control.						
UNIT – IV	BLDC MOTOR CONTROL	9				
Overview of BLDC Motor -Speed control methods -PWM techniques- ARM processor based BDLC motor control- ANN for BLDC Motor control and operation.						
UNIT - V	SRM MOTOR CONTROL	9				
Overview of SRM Motor -Speed control methods -PWM techniques- FPGA based SRM motor control- DNN for SRM Motor control and operation						
TOTAL: 45 PERIODS						


 Chairman (BoS)

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Interpret the significance of embedded control of electrical drives	Understand
CO2	Deliver insight into various control strategy for electrical drives.	Understand
CO3	Developing knowledge on Machine learning and optimization techniques for motor control.	Apply
CO4	Develop embedded system solution for real time application such as Electric vehicles and UAVs	Apply
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded system skills required for motor control strategy.	Apply

TEXT BOOKS:

1	R.Krishnan, "Electric Motor Drives – Modeling, Analysis and Control", Prentice-Hall of India Pvt. Ltd., New Delhi, 2010
2	Vedam Subramanyam, "Electric Drives – Concepts and Applications", Tata McGraw- Hill publishing company Ltd., New Delhi, 2002

REFERENCES:

1	K. Venkataratnam, Special Electrical Machines, Universities Press, 2014.
2	Steve Furber, 'ARM system on chip architecture', Addison Wesley, 2010.
3	Ron Sass and Andrew G. Schmidt, "Embedded System design with platform FPGAs: Principles and Practices", Elsevier, 2010.

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	-	2	-	2	-	-	-	-	1	-	3	-	2
CO2	1	1	3	-	-	2	-	-	-	1	-	3	-	2
CO3	2	-	-	-	3	-	-	-	-	1	-	3	-	2
CO4	1	2	3	1	-	-	-	-	-	1	-	3	-	2
CO5	-	-	-	-	3	-	-	-	-	1	-	3	-	2
Avg.	1.3	1.5	2.7	1	2.7	2	-	-	-	1	-	3	-	2


 Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1204	IoT FOR SMART SYSTEMS	Category	L	T	P	C
		PCC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> To study about Internet of Things technologies and its role in real time applications. To introduce the infrastructure required for IoT To familiarize the accessories and communication techniques for IoT. To provide insight about the embedded processor and sensors required for IoT To familiarize the different platforms and Attributes for IoT 						
UNIT - I	INTRODUCTION TO INTERNET OF THINGS	9				
Overview, Hardware and software requirements for IOT, Sensor and actuators, Technology drivers, Business drivers, Typical IoT applications, Trends and implications.						
UNIT - II	IOT ARCHITECTURE	9				
IoT reference model and architecture -Node Structure - Sensing, Processing, Communication, Powering, Networking - Topologies, Layer/Stack architecture, IoT standards, Cloud computing for IoT, Bluetooth, Bluetooth Low Energy beacons.						
UNIT - III	PROTOCOLS AND WIRELESS TECHNOLOGIES FOR IOT,PROTOCOLS	9				
NFC, SCADA and RFID, Zigbee MIPI, M-PHY, UniPro, SPMI, SPI, M-PCIe GSM, CDMA, LTE,GPRS, small cell. Wireless technologies for IoT: WiFi (IEEE 802.11), Bluetooth/Bluetooth Smart, ZigBee/ZigBee Smart, UWB (IEEE 802.15.4), 6LoWPAN, Proprietary systems-Recent trends.						
UNIT - IV	IOT PROCESSORS	9				
Services/Attributes: Big-Data Analytics for IOT, Dependability, Interoperability, Security, Maintainability. Embedded processors for IOT: Introduction to Python programming -Building IOT with RASPERRY PI and Arduino.						
UNIT - V	CASE STUDIES	9				
Industrial IoT, Home Automation, smart cities, Smart Grid, connected vehicles, electric vehicle charging, Environment, Agriculture, Productivity Applications, IOT Defense						
TOTAL: 45 PERIODS						


 Chairman (BoS)

COURSE OUTCOMES:		
Upon completion of the course, the students will be able to:		
Course Outcome	Description	Bloom's Taxonomy Level
CO1	Analyze the concepts of IoT and its present developments.	Analyze
CO2	Compare and contrast different platforms and infrastructures available for IoT.	Analyze
CO3	Explain different protocols and communication technologies used in IoT.	Understand
CO4	Analyze the big data analytic and programming of IoT	Analyze
CO5	Implement IoT solutions for smart applications	Apply
TEXT BOOKS:		
1	ArshdeepBahga and VijaiMadiseti : A Hands-on Approach "Internet of Things",UniversitiesPress 2015.	
2	Oliver Hersent , David Boswarthick and Omar Elloumi " The Internet of Things", Wiley,2016.	
REFERENCES:		
1	Samuel Greengard, " The Internet of Things", The MIT press, 2015.	
2	Adrian McEwen and Hakim Cassimally"Designing the Internet of Things "Wiley,2014.	
3	Jean- Philippe Vasseur, Adam Dunkels, "Interconnecting Smart Objects with IP: The NextInternet" Morgan Kuffmann Publishers, 2010.	

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	2	1	-	-	-	-	-	-	1	-	3	-	2
CO2	-	2	-	-	-	-	-	-	-	1	-	3	-	2
CO3	1	2	-	1	3	-	-	-	-	1	-	3	-	2
CO4	2		3	3	3	3	-	-	-	1	-	3	-	2
CO5	3	2	3	3	3	3	-	-	-	1	-	3	-	2
Avg.	1.8	2	2.3	2.3	3	2	-	-	-	1	-	3	-	2

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 Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1221	EMBEDDED SYSTEM LABORATORY - II	CATEGORY	L	T	P	C
		PCC	0	0	4	2
OBJECTIVES: The Course will enable learners to: <ul style="list-style-type: none"> ▪ To involve the students to Practice on Workbench /Software Tools/ HardwareProcessor Boards with the supporting Peripherals. ▪ To teach the concepts of algorithm development & programming on software tools andDigital processors with peripheral interfaces. ▪ To encourage students to practice in open source software's / packages /tools ▪ To train though hands-on practices in commercial and licensed Hardware-software suites ▪ Practicing through the subdivisions covered within experiments listed below to expose the students into the revising the concepts acquired from theory subjects. 						
LIST OF EXPERIMENTS					45	
<ul style="list-style-type: none"> • Programming ARM processor : ARM7 /ARM9/ARM Cortex <ul style="list-style-type: none"> - Study on In circuit Emulators, cross compilers, debuggers • I/O Programming with ARM processor : ARM7 / ARM9/ARM Cortex Microcontrollers I/O Interfacing : Timers/ Interrupts/ Serial port programming/PWM Generation/ Motor Control/ADC/DAC/ LCD/ RTC Interfacing/ Sensor Interfacing • Programming with Raspberry PiMicrocontroller Board : <ul style="list-style-type: none"> - Study on in circuit Emulators, cross compilers, debuggers • I/O Programming with Arduino ,Raspberry Pi Microcontroller Boards I/O Interfacing : Timers/ Interrupts/ Serial port programming/PWM Generation/ Motor Control/ADC/DAC/ LCD/ RTC Interfacing/ Sensor Interfacing/IoT Applications • Programming with DSP processors • Study of one type of Real Time OperatingSystems (RTOS) 						
EQUIPMENT/ SUPPORTS REQUIRED <ul style="list-style-type: none"> • Microcontrollers with peripherals; ;IDE, Board Support Software Tools /Keil/uCOS Compiler/others • ARM processor : ARM7 / ARM9/ARMCortex • Microcontrollers with peripherals; Board Support Software Tools, peripherals with interface • Rasberry Pi Boards with peripherals ;IDE,Board Support Software Tools • /Compiler/others • Arduino,Rasberry Pi Microcontroller Boardswith peripherals; Board Support Software Tools, peripherals with interface • Processor Boards with Board Support Tools& Interfaces Compilers & Platforms with VXWorks/ Keil/ Android/ Tiny OS/ Linux Support/any RTOS/Java Semaphore implementations 						
TOTAL: 45 PERIODS						

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Experiment and demonstrate with simulators, in programming processor boards, processor interfacing/ designing digital controllers	Apply
CO2	Design & simulate Arithmetic ,Logic programs, Filters, Signal analysis with simulators/experiments ,in programming processor boards, processor interfacing/ Tools	Apply
CO3	Develop real time solution for embedded applications.	Create
CO4	Program and compile in various tools & software domains.	Apply
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in commercial embedded processors and its programmable interfacing.	Apply

TEXT BOOKS:

1	Mohammad Ali Mazidi&Mazidi ' 8051 Microcontroller and Embedded Systems', Pearson Education
2	Simon Monk," Make Action-with Arduino and Raspberry Pi,SPD ,2016

REFERENCES:

1	Taan S.Elali,"Discrete Systems and Digital Signal Processing with Matlab",CRC Press2009.
2	JovithaJerome,"Virtual Instrumentation using Labview"PHI,2010.
3	Woon-Seng Gan, Sen M. Kuo, 'Embedded Signal Processing with the Micro Signal Architecture',John Wiley & Sons, Inc., Hoboken, New Jersey 2007

Mapping of COs with POs and PSOs

COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	3	1	1	2	1	-	-	-	1	-	3	-	2
CO2	-	1	2	-	-	-	-	-	-	1	-	3	-	2
CO3	1	-	3	2	3	-	-	-	-	1	-	3	-	2
CO4	2	2	3	3	3	3	-	-	-	1	-	3	-	2
CO5	3	2	3	3	3	3	-	-	-	1	-	3	-	2
Avg.	1.75	2	2.4	2.25	2.75	1.75	-	-	-	1	-	3	-	2

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Chairman (BOS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
0	0	4	2	Laboratory only (60%)	Laboratory only (40%)
LABORATORY					
Evaluation Laboratory Record			Model Practical		Max CIE Marks
75*			25*		100*
Total Marks shall be converted in to 60					


Chairman (BoS)

23ET1222	EMBEDDED PROGRAMMING LABORATORY – II	Category	L	T	P	C
		PCC	0	0	4	2
<p>OBJECTIVES:</p> <p>The Course will enable learners to:</p> <ul style="list-style-type: none"> To involve the students to Practice on Workbench /Software Tools/ Hardware ProcessorBoards with the supporting Peripherals. To teach the concepts of algorithm development & programming on software tools andDigital processors with peripheral interfaces. To encourage students to practice in open source software / packages /tools To train though hands-on practices in commercial and licensed Hardware-software suites Practicing through the subdivisions covered within experiments listed below to expose the students into the revising the concepts acquired from theory subjects. 						
LIST OF EXPERIMENTS					60	
<p>Programming in Freeware software's/ Platforms</p> <p>Software & Modelling tools</p> <ul style="list-style-type: none"> ✓ Study on MEMS Tools ✓ Study on process Controller modeling ✓ PLC/SCADA/PCB ✓ one type CAD Tool • Programming & Simulation in GUI Simulators /Tools/others • Graphical User interface simulations & modeling of instrumentation & controllers • Programming & Simulation in Python Simulators/Tools/others • Programming with wired/wireless communication protocol/Network Simulators • Linux programming Tool chain <p>EQUIPMENT/ SUPPORTS REQUIRED</p> <ul style="list-style-type: none"> • Programming Compilers & Platforms onfreeware Simulation Tools as MATLAB /others • Personal Computers, • Software & programming/modelling tools • Simulation Tools as LabVIEW /others • Programming in Python Platform • Learning Communication Protocols & Support Software Tools for BUS & network communication • PC with Linux OS 						
TOTAL: 60 PERIODS						


Chairman (BoS)

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Developing Optimized algorithms for embedded processor on IDE and compilers.	Apply
CO2	Outline the concepts of how process can be realized using Software Modules.	Apply
CO3	Compare and analyze device, Circuit and System level simulators/emulators to develop embedded applications.	Apply
CO4	Incorporate I/O software interface using IDE and High level languages with processor	Apply
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on Embedded programming concepts.	Apply

TEXT BOOKS:

1	Mohammad Ali Mazidi & Mazidi ' 8051 Microcontroller and Embedded Systems', Pearson Education
2	Simon Monk, " Make Action-with Arduino and Raspberry Pi, SPD ,2016

REFERENCES:

1	Taan S.Elali, "Discrete Systems and Digital Signal Processing with Matlab", CRC Press 2009.
2	Jovitha Jerome, "Virtual Instrumentation using Labview" PHI, 2010.
3	Woon-Seng Gan, Sen M. Kuo, 'Embedded Signal Processing with the Micro Signal Architecture', John Wiley & Sons, Inc., Hoboken, New Jersey 2007

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	1	1	2	1	-	-	-	1	-	3	-	2
CO2	-	3	2	2	-	-	-	-	-	1	-	3	-	2
CO3	2	3	3	2	3	2	-	-	-	1	-	3	-	2
CO4	-	1	3	3	3	3	-	-	-	1	-	3	-	2
CO5	-	-	3	3	3	3	-	-	-	1	-	3	-	2
Avg.	2	2.25	2.4	2.2	2.75	2.25	-	-	-	1	-	3	-	2

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Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
0	0	4	2	Laboratory only (60%)	Laboratory only (40%)
LABORATORY					
Evaluation Laboratory Record			Model Practical		Max CIE Marks
75*			25*		100*
Total Marks shall be converted in to 60					


Chairman (BoS)

23ET1P01	WIRELESS AND MOBILE COMMUNICATION	Category	L	T	P	C
		PEC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> • To study the Channel planning for Wireless Systems • To study the Mobile Radio Propagation and Equalization and Diversity • To study the Equalization and Diversity • To provide insight about wideband code division based access. • To study the Wireless multiple access and IP 						
UNIT - I	THE CELLULAR CONCEPT	9				
System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies-Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity –Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference, Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems-Cell Splitting, Sectoring.						
UNIT - II	MOBILE RADIO PROPAGATION: LARGE-SCALE PATH LOSS	9				
Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, Diffraction-Fresnel Zone Geometry, Knife edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models-Longley-Ryce Model, Okumura Model, Hata Model, Indoor Propagation Models-Partition losses, Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modelling.						
UNIT - III	MOBILE RADIO PROPAGATION	9				
Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel-Relationship between Bandwidth and Received power, Small-Scale Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Nonlinear Equalization						
UNIT – IV	WIDEBAND CODE DIVISION MULTIPLE ACCESS	9				
CDMA system overview -air interface –physical and logical channel–speech coding, multiplexing and channel coding –spreading and modulation: frame structure, spreading codes-uplink-downlink – physical layer procedures: cell search and synchronization-establishing a connection-power control-handover-overload control.						
UNIT - V	IP MOBILITY FRAMEWORK	9				
Challenges of IP Mobility -Address Management -Dynamic Host Configuration Protocol and Domain Name Server Interfaces –Security –Mobility-Based AAA Protocol -IP Mobility Architecture Framework-x Access Network -IPv6 Challenges for IP Mobility.						
TOTAL: 45 PERIODS						

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Cellular communication concepts.	Understand
CO2	Explain the mobile radio propagation.	Understand
CO3	Perceive the wireless network different type of MAC protocols	Apply
CO4	Analyze the Equalization and Diversity	Analyze
CO5	Build the Wireless multiple access and IP	Apply

TEXT BOOKS:

- 1 | Wireless Communications, Principles, Practice –Theodore, S. Rappaport, 2nd Ed., 2002, PHI.
- 2 | Wireless Communications Andrea Goldsmith, 2005 Cambridge University Press.

REFERENCES:

- 1 | Principles of Wireless Networks –KavehPahLaven and P. Krishna Murthy, 2002, PE
- 2 | Mobile Cellular Communication –GottapuSasibhushana Rao, Pearson Education, 2012.
- 3 | Wireless Digital Communications –Kamilofeher, 1999, PHI.

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	1	-	-	-	-	-	1	-	3	-	2
CO2	3	3	2	2	-	-	-	-	-	1	-	3	-	2
CO3	3	3	2	3	2	2	-	-	-	1	-	3	-	2
CO4	2	2	2	2	2	2	-	-	-	1	-	3	-	2
CO5	2	2	2	2	2	2	-	-	-	1	-	3	-	2
Avg.	2.6	2.6	2	2	2	2	-	-	-	1	-	3	-	2

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Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1P02	VIRTUAL INSTRUMENTATION	Category	L	T	P	C
		PEC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> • Understanding the difference between conventional and graphical programming. • Introducing the basics of Lab VIEW and programming concepts. • Differentiating the real time and virtual instrument. • Represent and review signals acquire process in digital domain. • Analyzing the basics of data acquisition and learning the concepts of data acquisition with LabVIEW 						
UNIT - I	FUNDAMENTALS OF VIRTUAL INSTRUMENTATION	9				
Fundamental Concepts of Virtual Instrumentation (VI) and Graphical Programming - Virtual instruments and Traditional instruments, Hardware and Software in virtual instrumentation, Data Flow Programming-Data Types – Customization of VI Properties - VI Documentation.						
UNIT - II	VI PROGRAMMING STRUCTURES	9				
Software Environment - Modular programming - Formula Nodes - Loops - Shift Registers - Local and Global Variables – Case and Sequence Structures - Arrays and Clusters - Graphs and Charts - State Machines - String and File I/O.						
UNIT - III	DATA ACQUISITION AND INTERFACING STANDARDS	9				
PC based data acquisition – DAQ hardware and software architecture – DAQ hardware configuration, sampling methods and grounding techniques, analog I/O, digital I/O, counter/timer - Communication: Interfacing of external instruments to a PC - RS232 - RS485 - GPIB – System Interface Buses: USB-PCI, PXI; Introduction to bus protocols of MOD bus and CAN bus - Industrial Ethernet.						
UNIT – IV	ADVANCED PROGRAMMING	9				
Introduction, Definition of State Machine, A Simple State Machine, Event Structures. File Input / Output: Introduction, File Formats, File I/O Functions, Path Functions, Sample VIs to Demonstrate File WRITE and READ Function String Handling: Introduction, String Functions, Lab VIEW String Formats, Typical examples Use of analysis tools and application of VI: Fourier transforms, Power spectrum, Simulation of systems using VI: Development of Control system, Image acquisition and processing.						
UNIT - V	CASE STUDIES	9				
Temperature Monitoring System using PC based Data Acquisition System - Machine vision, Motion control, Configuration of Real-Time I/O Hardware in MAX - Host & Target VI – Prioritization of Tasks – Timed Programming Structures in Lab VIEW – Real-Time Application Deployment using my RIO – Run-time Interaction with Deployed Applications – Running Web Services in my RIO.						
TOTAL: 45 PERIODS						


 Chairman (BoS)

COURSE OUTCOMES:		
Upon completion of the course, the students will be able to:		
Course Outcome	Description	Bloom's Taxonomy Level
CO1	Infer and Interpret the fundamentals of Virtual Instrumentation and dataAcquisition.	Understand
CO2	Explain the difference between the traditional and virtual instrumentation.	Understand
CO3	Illustrate the theoretical concepts to realize practical systems.	Apply
CO4	Analyze and evaluate the performance of Virtual Instrumentation Systems	Analyze
CO5	Build a VI system to solve real time problems using data acquisition.	Apply
TEXT BOOKS:		
1	Jovitha Jerome, —Virtual Instrumentation using Lab VIEWI, PHI Learning Pvt. Ltd.,2010.	
2	Sanjay Gupta and Joseph John, “Virtual Instrumentation Using Lab VIEW”, TataMcGraw Hill, 2008.	
REFERENCES:		
1	Gary Johnson and Richard Jennings, —Lab VIEW Graphical ProgrammingI, McGraw Hill Inc., Fourth Edition, 2006	
2	Rick Bitter, Taqi Mohiuddin and Matt Nawrocki, “Lab VIEW Advanced Programming Techniques”, CRC Press, 2009.	
3	Lisa. K. Wills, “Lab VIEW for Everyone”, Prentice Hall of India, 2nd Edition, 2008.	

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	2	1	2	-	-	-	-	-	1	-	3	-	2
CO2	-	-	2	-	-	-	-	-	-	1	-	3	-	2
CO3	1	3	3	3	1	1	-	-	-	1	-	3	-	2
CO4	2	2	3	3	2	2	-	-	-	1	-	3	-	2
CO5	3	3	3	3	3	3	-	-	-	1	-	3	-	2
Avg.	2	2.5	2.4	2.75	2	2	-	-	-	1	-	3	-	2

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 Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1P03	EMBEDDED PROCESSOR DEVELOPMENT	Category	L	T	P	C
		PEC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> • To learn about basic concepts of embedded system • To learn about ARM architecture • To learn C language and assembly programming. • To learn Object orientation for programming and C++. • To learn software modelling fundamentals 						
UNIT - I	EMBEDDED CONCEPTS	9				
Introduction to embedded systems, Application Areas, Categories of embedded systems, Overview of embedded system architecture, Specialties of embedded systems, recent trends in embedded systems, Architecture of embedded systems, Hardware architecture, Software architecture, Application Software, Communication Software, Development and debugging Tools.						
UNIT - II	ARM ARCHITECTURE AND OVERVIEW OF CORTEX	9				
Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture. Overview of Cortex-M3. Cortex-M3 Basics: Registers, General Purpose Registers, Stack Pointer, Link Register, ProgramCounter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector. Tables, Stack Memory Operations, Reset Sequence. Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions. Cortex-M3 Implementation Overview: Pipeline, Block Diagram, BusInterfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus.						
UNIT - III	CORTEX-M3/M4 PROGRAMMING	9				
Overview, Typical Development Flow, Using C, CMSIS (Cortex Microcontroller Software Interface Standard), Using Assembly Exception Programming: Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Vector Table Relocation. Memory Protection Unit and other Cortex-M3 features: MPU Registers, Setting Up the MPU, Power Management, Multiprocessor Communication.						
UNIT - IV	UNIFIED MODELING LANGUAGE	9				
Connecting the object model with the use case model – Key strategies for object identification – UMLbasics. Object state behaviour – UML state charts – Role of scenarios in the definition of behaviour –Timing diagrams – Sequence diagrams – Event hierarchies – types and strategies of operations – Architectural design in UML concurrency design – threads in UML.						
UNIT - V	EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS	9				
The compilation process – libraries – porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS - system design using RTOS						
TOTAL: 45 PERIODS						

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Demonstrate about basic concepts of embedded system	Understand
CO2	Build ARM architecture	Understand
CO3	Understand C language and assembly programming.	Apply
CO4	Build and compile Object orientation for programming and C++.	Apply
CO5	Create software modelling	Apply

TEXT BOOKS:

1	David Seal "ARM Architecture Reference Manual", 2001 Addison Wesley, England; MorganKaufmann Publishers
2	Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide -Designingand Optimizing System Software", 2006, Elsevier.

REFERENCES:

1	Cortex-M series-ARM Reference Manual .
2	Ajay Deshmukh, "Microcontroller -Theory & Applications", Tata McGraw Hill.
3	The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, econd Edition, Elsevier Inc. 2010.

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	3	1	1	-	3	-	-	-	1	-	3	-	2
CO2	3	-	3	3	2	-	-	-	-	1	-	3	-	2
CO3	-	-	2	2	3	-	-	-	-	1	-	3	-	2
CO4	-	-	3	-	3	-	-	-	-	1	-	3	-	2
CO5	2	-	3	2	3	-	-	-	-	1	-	3	-	2
Avg.	2.3	3	2.4	2	2.7	3	-	-	-	1	-	3	-	2

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Chairman (BoS)

(BoS) Chairman

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1P04	AUTOMOTIVE EMBEDDED SYSTEM	Category	L	T	P	C
		PEC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> To expose the students to the fundamentals and building of Electronic Engine Controlsystems. To teach on functional components and circuits for vehicles. To discuss on programmable controllers for vehicles management systems. To teach logics of automation & commercial techniques for vehicle communication. To introduce the embedded systems concepts for E-vehicle system development. 						
UNIT - I	BASIC OF ELECTRONIC ENGINE CONTROL SYSTEMS	9				
Overview of Automotive systems, fuel economy, air-fuel ratio, emission limits and vehicle performance; Automotive microcontrollers- Electronic control Unit- Hardware & software selection and requirements for Automotive applications — open source ECU- RTOS - Concept for Engine management-Standards; Introduction to AUTOSAR and Introduction to Society SAE- Functional safety ISO 26262- Simulation and modeling of automotive system components.						
UNIT - II	SENSORS AND ACTUATORS FOR AUTOMOTIVES	9				
Review of sensors- sensors interface to the ECU, conventional sensors and actuators, Modern sensor and actuators - LIDAR sensor- smart sensors- MEMS/NEMS sensors and actuators for automotive applications.						
UNIT - III	VEHICLE MANAGEMENT SYSTEMS	9				
Electronic Engine Control-engine mapping, air/fuel ratio spark timing control strategy, fuel control, electronic ignition- Adaptive cruise control - speed control-anti-locking braking system-electronic suspension - electronic steering , Automatic wiper control- body control system ; Vehicle system schematic for interfacing with EMS, ECU. Energy Management system for electric vehicles- Battery management system , power management system-electrically assisted power steering system- Adaptive lighting system- Safety and Collision Avoidance						
UNIT – IV	ONBOARD DIAGONSTICS AND TELEMATICS	9				
On board diagnosis of vehicles -System diagnostic standards and regulation requirements Vehicle communication protocols Bluetooth, CAN, LIN, FLEXRAY, MOST, KWP2000 and recent trends in vehicle communications- Navigation- Connected Cars technology — Tracking- Security for data communication- dashboard display and Virtual Instrumentation, multimedia electronics- Role of IOT in Automotive systems						
UNIT - V	ELECTRIC VEHICLES	9				
Electric vehicles –Components- Plug in Electrical vehicle- Charging station — Aggregators- Fuel cells/Solar powered vehicles- Autonomous vehicles.						
TOTAL: 45 PERIODS						

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Insight into the significance of the role of embedded system for automotive applications.	Understand
CO2	Illustrate the need, selection of sensors and actuators and interfacing with ECU	Apply
CO3	Develop the Embedded concepts for vehicle management and control systems.	Apply
CO4	Demonstrate the need of Electrical vehicle and able to apply the embedded system technology for various aspects of EVs	Apply
CO5	Improved Employability and entrepreneurship capacity due to knowledge up gradation on recent trends in embedded systems design and its application in automotive systems.	Apply

TEXT BOOKS:

1	William B. Ribbens ,”Understanding Automotive Electronics”, Elseiver,2012
2	Ali Emedi, Mehrdedehsani, John M Miller , “Vehicular Electric power system- land, Sea, Air and Space Vehicles” Marcel Decker, 2004.

REFERENCES:

1	L.Vlacic,M.Parent,F.Harahima,”Intelligent Vehicl Technologies” ,SAE International,2001.
2	Ajay Deshmukh, “Microcontroller -Theory & Applications”, Tata McGraw Hill.
3	Jack Erjavec,JeffArias,”Alternate Fuel Technology-Electric ,Hybrid&Fuel Cell Vehicles”,Cengage ,2012.

Mapping of COs with POs and PSOs

COs / POs	PO 1	PO2	PO 3	PO4	PO 5	PO6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO2
CO1	-	2	1	1	-	2	-	-	-	1	-	3	-	2
CO2	2	3	2	2	2	3	-	-	-	1	-	3	-	2
CO3	3	3	3	3	3	2	-	-	-	1	-	3	-	2
CO4	3	3	3	3	3	2	-	-	-	1	-	3	-	2
CO5	3	3	3	3	3	2	-	-	-	1	-	3	-	2
Avg.	2.7	2.8	2.4	2.4	2.7	2.2	-	-	-	1	-	3	-	2

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Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1P 05	INTELLIGENT CONTROL AND AUTOMATION	Category	L	T	P	C
		PEC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> • To Impart the knowledge of various optimization techniques and hybrid schemes. • To introduce the concept, Analysis and implementation of ANN and Fuzzy logic controllers. • To Emphasis the need for Genetic algorithm and its role for automation. • To provide the basics of automation and its requirements • To demonstrate the role of Intelligent controller in automation applications. 						
UNIT - I	ARTIFICIAL NEURAL NETWORK & FUZZY LOGIC	9				
ARTIFICIAL NEURAL NETWORK: Learning with ANNs, single-layer networks, multi-layer perceptron's, Back propagation algorithm (BPA) ANNs for identification, ANNs for control, Adaptive neuro controller. Fuzzy Logic Control: Introduction, fuzzy sets, fuzzy logic, fuzzy logic controller design, Fuzzy Modelling & identification, Adaptive Fuzzy Control Design.						
UNIT - II	GENETIC ALGORITHM	9				
Basic concept of Genetic algorithm and detail algorithmic steps- Hybrid genetic algorithm - Solution for typical control problems using genetic algorithm. Concept on some other search techniques like Tabu search, Ant-colony search and Particle Swarm Optimization						
UNIT - III	HYBRID CONTROL SCHEMES	9				
Fuzzification and rule base using ANN-Neuro fuzzy systems-ANFIS-Optimization of membership function and rule base using Genetic Algorithm and Particle Swarm Optimization						
UNIT - IV	AUTOMATION	9				
Introduction to Automation - Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations- Industrial Automation -computer vision for automation- PLC and SCADA based Automation- IoT for automation- Industry 4.0.						
UNIT - V	INTELLIGENT CONTROLLER FOR AUTOMATION APPLICATION	9				
Applications of Intelligent controllers in Industrial Monitoring, optimization and control- Smart Appliances- Automation concept for Electrical vehicle- Intelligent controller and Automation for Power System.						
TOTAL: 45 PERIODS						


Chairman (BoS)

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Demonstrate the basic architectures of NN and Fuzzy logics	Understand
CO2	Design and implement GA algorithms and know their limitations	Apply
CO3	Explain and evaluate hybrid control schemes	Apply
CO4	Interpret the significance of Automation concepts.	Apply
CO5	Develop the intelligent controller for automation applications.	Apply

TEXT BOOKS:

1	Laurene V.Fausett, "Fundamentals of Neural Networks, Architecture, Algorithms, and Applications", Pearson Education, 2008.
2	Timothy J.Ross, "Fuzzy Logic with Engineering Applications", Wiley, Third Edition, 2010.

REFERENCES:

1	David E.Goldberg, "Genetic Algorithms in Search, Optimization, and Machine Learning", Pearson Education, 2009.
2	W.T.Miller, R.S.Sutton and P.J.Webrose, "Neural Networks for Control", MIT Press, 1996.
3	ChanchalDey and Sunit Kumar Sen, Industrial Automation Technologies, 1st Edition, CRC Press, 2022.

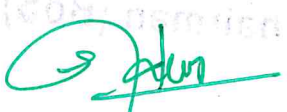
Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	1	1	1	-	1	-	-	-	1	-	3	-	2
CO2	2	2	3	3	3	2	-	-	-	1	-	3	-	2
CO3	3	2	2	2	-	-	-	-	-	1	-	3	-	2
CO4	3	2	2	2	-	-	-	-	-	1	-	3	-	2
CO5	3	-	3	3	-	2	-	-	-	1	-	3	-	2
Avg.	2.4	1.7	2.2	2.2	3	1.7	-	-	-	1	-	3	-	2


Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


 Chairman (BoS)

23ET1P06	UNMANNED AERIAL VEHICLE	Category	L	T	P	C
		PEC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ol style="list-style-type: none"> 1. To make the students to understand the basic concepts and components of UAV systems. 2. To teach the UAV design concepts. 3. To provide an insight about the hardware structure for UAVs. 4. To emphasis the communication protocol requirements and control strategy for UAVs. 5. To highlight the need and the role of UAVs for real time applications and development of realtime UAVs. 						
UNIT - I	INTRODUCTION TO UAV	9				
Overview and background - History of UAV –classification – societal impact and future outlook Unmanned Aerial System (UAS) components --models and prototypes – System Composition- applications						
UNIT - II	THE DESIGN OF UAV SYSTEMS	9				
Introduction to Design and Selection of the System- Aerodynamics and Airframe Configurations- Characteristics of Aircraft Types- Design Standards-Regulatories and regulations - Design for Stealth--control surfaces-specifications.						
UNIT - III	HARDWAREs for UAVs	9				
Real time Embedded processors for UAVs - sensors-servos-accelerometer –gyros-actuators-power supply- integration, installation, configuration, and testing –MEMS/NEMS sensors and actuators for UAVs- Autopilot – AGL.						
UNIT – IV	COMMUNICATION PAYLOADS AND CONTROLS	9				
Payloads-Telemetry-tracking-Aerial photography-controls-PID feedback-radio control frequency range –modems-memory system-simulation-ground test-analysis-trouble shooting.						
UNIT - V	THE DEVELOPMENT OF UAV SYSTEMS	9				
Waypoints navigation-ground control software- System Ground Testing- System In-flight Testing- Mini, Micro and Nano UAVs- Case study: Agriculture- Health- Surveying- Disaster Management and Defense.						
TOTAL: 45 PERIODS						


Chairman (BoS)

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Identify different hardware for UAV	Understand
CO2	Determine preliminary design requirements for an unmanned aerial vehicle	Apply
CO3	Design UAV system.	Apply
CO4	Identify and Integrate various systems of unmanned aerial vehicle.	Apply
CO5	Design micro aerial vehicle systems by considering practical limitations	Apply

TEXT BOOKS:

1	Reg Austin "Unmanned Aircraft Systems UAV design, development and deployment", Wiley, 2010.
2	Paul G Fahlstrom, Thomas J Gleason, "Introduction to UAV Systems", UAV Systems, Inc, 1998

REFERENCES:


1	Dr. Armand J. Chaput, "Design of Unmanned Air Vehicle Systems", Lockheed Martin Aeronautics Company, 2001
2	Kimon P. Valavanis, "Advances in Unmanned Aerial Vehicles: State of the Art and the Road to Autonomy", Springer, 2007
3	Robert C. Nelson, Flight Stability and Automatic Control, McGraw-Hill, Inc, 1998.

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	3	2	-	-	2	-	-	-	1	-	3	-	2
CO2	3	3	3	-	-	2	-	-	-	1	-	3	-	2
CO3	3	3	3	3	3	3	-	-	-	1	-	3	-	2
CO4	-	-	2	3	3	2	-	-	-	1	-	3	-	2
CO5	3	-	3	3	3	3	-	-	-	1	-	3	-	2
Avg.	2.5	3	2.6	3	3	2.4	-	-	-	1	-	3	-	2


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Chairman (BoS)

ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


Chairman (BoS)

23ET1P07	DSP BASED SYSTEM DESIGN	Category	L	T	P	C
		PEC	3	0	0	3
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> • To understand various representation methods of DSP system • To provide insight about different DSP algorithms • To familiarize the various architectures of DSP system • To perform analysis of DSP architectures and to learn the implementation of DSP system inprogrammable hardware • To learn the details of DSP system interfacing with other peripherals 						
UNIT - I	REPRESENTATION OF DSP SYSTEM	9				
Single Core and Multicore, Architectural requirement of DSPs - high throughput, low cost, low power, small code size, embedded applications. Representation of digital signal processing systems - block diagrams, signal flow graphs, data-flow graphs, dependence graphs. Techniques for enhancing computational throughput - parallelism and pipelining.						
UNIT - II	DSP ALGORITHMS	9				
DSP algorithms - Convolution, Correlation, FIR/IIR filters, FFT, adaptive filters, sampling rate converters, DCT, Decimator, Expander and Filter Banks. DSP applications. Computational characteristics of DSP algorithms and applications, Numerical representation of signals-word length effect and its impact, Carry free adders, Multiplier.						
UNIT - III	SYSTEM ARCHITECTURE	9				
Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing. VLIW architecture. Basic performance issue in pipelining, Simple implementation of MIPS, Instruction Level Parallelism, Dynamic Scheduling, Dynamic Hardware Prediction, Memory hierarchy. Study of Fixed point and floating point DSP architectures						
UNIT - IV	ARCHITECTURE ANALYSIS ON PROGRAMMABLE HARDWARE	9				
Analysis of basic DSP Architectures on programmable hardware's. Algorithms for FIR , IIR, Latticefilter structures, architectures for real and complex fast Fourier transforms, 1D/2D Convolutions, Winograd minimal filtering algorithm. FPGA: Architecture, different sub-systems, design flow for DSP system design, mapping of DSP algorithms onto FPGA.						
UNIT - V	SYSTEM INTERFACING	9				
Examples of digital signal processing algorithms suitable for parallel architectures such as GPUs and multiGPUs. Interfacing: Introduction, Synchronous Serial Interface CODE, A CODEC Interface Circuit, ADC interface.						
TOTAL: 45 PERIODS						


Chairman (BoS)

COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Evaluate the DSP system using various methods	Understand
CO2	Design algorithm suitable for different DSP applications	Apply
CO3	Explain various architectures of DSP system	Apply
CO4	Implement DSP system in programmable hardware.	Apply
CO5	Interfacing of DSP system with various peripherals	Apply

TEXT BOOKS:

1	Digital Signal Processing and Application with C6713 and C6416 DSK, Rulph Chassaing, Worcester Polytechnic Institute, A Wiley Interscience Publication
2	Architectures for Digital Signal Processing, Peter Pirsch John Wiley, 2007

REFERENCES:

1	Sen M Kuo, Woon Seng S Gan, Digital Signal Processors
2	Nasser Kehtarnavaz, Digital Signal Processing System Design: LabVIEW-Based Hybrid Programming, Academic Press, 2008
3	Keshab K Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, student Edition, Wiley, 1999.

Mapping of COs with POs and PSOs

COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	3	-	-	-	-	-	-	-	1	-	3	-	2
CO2	3	3	3	2	3	2	-	-	-	1	-	3	-	2
CO3	-	3	-	-	-	-	-	-	-	1	-	3	-	2
CO4	3	-	3	3	3	3	-	-	-	1	-	3	-	2
CO5	2	-	3	2	3	3	-	-	-	1	-	3	-	2
Avg.	2.6	3	3	2.3	3	2.7	-	-	-	1	-	3	-	2

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ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE- 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


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23ET1P08	MACHINE LEARNING AND DEEP LEARNING	Category	L	T	P	C
		PEC	3	0	0	3
OBJECTIVES: The Course will enable learners to: <ul style="list-style-type: none"> • Understanding about the learning problem and algorithms • Providing insight about neural networks • Introducing the machine learning fundamentals and significance • Enabling the students to acquire knowledge about pattern recognition. • Motivating the students to apply deep learning algorithms for solving real life problems. 						
UNIT - I	LEARNING PROBLEMS AND ALGORITHMS	9				
Various paradigms of learning problems, Supervised, Semi-supervised and Unsupervised algorithms.						
UNIT - II	NEURAL NETWORKS	9				
Differences between Biological and Artificial Neural Networks - Typical Architecture, Common Activation Functions, Multi-layer neural network, Linear Separability, Hebb Net, Perceptron, Adaline, Standard Back propagation Training Algorithms for Pattern Association - Hebb rule and Delta rule, Hetero associative, Auto associative, Kohonen Self Organizing Maps, Examples of Feature Maps, Learning Vector Quantization, Gradient descent, Boltzmann Machine Learning.						
UNIT - III	MACHINE LEARNING – FUNDAMENTALS & FEATURE SELECTIONS & CLASSIFICATIONS	9				
Classifying Samples: The confusion matrix, Accuracy, Precision, Recall, F1- Score, the curse of dimensionality, training, testing, validation, cross validation, overfitting, under-fitting the data, early stopping, regularization, bias and variance. Feature Selection, normalization, dimensionality reduction, Classifiers: KNN, SVM, Decision trees, Naïve Bayes, Binary classification, multi class classification, clustering						
UNIT – IV	DEEP LEARNING: CONVOLUTIONAL NEURAL NETWORKS	9				
Feed forward networks, Activation functions, back propagation in CNN, optimizers, batch normalization, convolution layers, pooling layers, fully connected layers, dropout, Examples of CNNs..						
UNIT - V	DEEP LEARNING: RNNs, AUTOENCODERS AND GANS	9				
State, Structure of RNN Cell, LSTM and GRU, Time distributed layers, Generating Text, Autoencoders: Convolutional Autoencoders, Denoising autoencoders, Variational autoencoders, GANs: The discriminator, generator, DCGANs						
TOTAL: 45 PERIODS						

COURSE OUTCOMES:		
Upon completion of the course, the students will be able to:		
Course Outcome	Description	Bloom's Taxonomy Level
CO1	Illustrate the categorization of machine learning algorithms	Understand
CO2	Compare and contrast the types of neural network architectures, activation functions	Apply
CO3	: Acquaint with the pattern association using neural networks	Apply
CO4	laborate various terminologies related with pattern recognition and architectures ofconvolutional neural networks	Apply
CO5	Construct different feature selection and classification techniques and advanced neuralnetwork architectures such as RNN, Autoencoders, and GANs.	Apply
TEXT BOOKS:		
1	J. S. R. Jang, C. T. Sun, E. Mizutani, Neuro Fuzzy and Soft Computing - A ComputationalApproach to Learning and Machine Intelligence, 2012, PHI learning	
2	Deep Learning, Ian Good fellow, YoshuaBengio and Aaron Courville, MIT Press, ISBN:9780262035613, 2016.	
REFERENCES:		
1	The Elements of Statistical Learning. Trevor Hastie, Robert Tibshirani and Jerome Friedman.Second Edition. 2009.	
2	Pattern Recognition and Machine Learning. Christopher Bishop. Springer. 2006. Understanding Machine Learning. Shai Shalev-Shwartz and Shai Ben-David. CambridgeUniversity Press. 2017	

Mapping of COs with POs and PSOs														
COs/ POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1	3	1	-	-	1	-	-	-	1	-	3	-	2
CO2	2	3	2	-	-	2	-	-	-	1	-	3	-	2
CO3	3	-	3	-	3	3	-	-	-	1	-	3	-	2
CO4	2	3	3	-	-	2	-	-	-	1	-	3	-	2
CO5	3	3	3	-	3	3	-	-	-	1	-	3	-	2
Avg.	2.2	3	2.4	-	3	2.2	-	-	-	1	-	3	-	2


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ASSESSMENT SYSTEM:					
L	T	P	C	Continuous Internal Examination (CIE)	End Semester Examination (ESE)
3	0	0	3	Theory only (40%)	Theory only (60%)
CONTINUOUS INTERNAL EXAMINATION :					
THEORY					
Assessment	Portions	Duration	Max. Mark	Max CIE Marks	
CIE - 1	2.5 units	3 Hours	100	Best 2 out of 3 and Converted to 60	
CIE - 2	2.5 units	3 Hours	100		
Improvement / Missed Test	2.5 units	3 Hours	100		
Other Assessment Methods	Quizzes (10 MCQ per unit)		20	40	
	Assignment / Case Study / Seminar / Tutorial / Mini Project / Open Book Test		20		
				100	
*The weighted average shall be converted into 40 marks for internal assessment.					


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23AC1131	ENGLISH FOR RESEARCH PAPER WRITING	Category	L	T	P	C
		AC	2	0	0	0
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> • Teach how to improve writing skills and level of readability • Tell about what to write in each section • Summarize the skills needed when writing a Title • Infer the skills needed when writing the Conclusion • Ensure the quality of paper at very first-time submission 						
UNIT - I	INTRODUCTION TO RESEARCH PAPER WRITING	6				
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness						
UNIT - II	PRESENTATION SKILLS	6				
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction						
UNIT - III	TITLE WRITING SKILLS	6				
Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check						
UNIT - IV	RESULT WRITING SKILLS	6				
Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions						
UNIT - V	VERIFICATION SKILLS	6				
Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first time submission						
TOTAL: 30 PERIODS						
COURSE OUTCOMES:						
Upon completion of the course, the students will be able to:						
Course Outcome	Description	Bloom's Taxonomy Level				
CO1	Understand that how to improve your writing skills and level of readability	Understand				
CO2	Learn about what to write in each section	Understand				
CO3	Understand the skills needed when writing a Title	Understand				
CO4	Understand the skills needed when writing the Conclusion	Understand				
CO5	Ensure the good quality of paper at very first-time submission	Understand				


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REFERENCES:	
1	Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2	Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3	Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4	Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.


Chairman (BOS)

23AC1132	DISASTER MANAGEMENT	Category	L	T	P	C
		AC	2	0	0	0
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> Summarize basics of disaster. Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response. Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives. Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations. Develop the strengths and weaknesses of disaster management approaches 						
UNIT - I	INTRODUCTION	6				
Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.						
UNIT - II	REPERCUSSIONS OF DISASTERS AND HAZARDS	6				
Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.						
UNIT - III	DISASTER PRONE AREAS IN INDIA	6				
Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics						
UNIT - IV	DISASTER PREPAREDNESS AND MANAGEMENT	6				
Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.						
UNIT - V	RISK ASSESSMENT	6				
Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival						
TOTAL: 30 PERIODS						


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COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Ability to summarize basics of disaster	Understand
CO2	Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.	Understand
CO3	Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives	Understand
CO4	Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.	Understand
CO5	Ability to develop the strengths and weaknesses of disaster management approaches	Understand

REFERENCES:

1	Goel S. L., Disaster Administration And Management Text And Case Studies", Deep& Deep Publication Pvt. Ltd., New Delhi,2009.
2	NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies ""NewRoyal book Company,2007.
3	Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi,2001.


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23AC1133	CONSTITUTION OF INDIA	Category	L	T	P	C
		AC	2	0	0	0
OBJECTIVES:						
The Course will enable learners to:						
<ul style="list-style-type: none"> • Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective. • To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional • Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism. • To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution. 						
UNIT - I	HISTORY OF MAKING OF THE INDIAN CONSTITUTION	6				
History, Drafting Committee, (Composition & Working)						
UNIT - II	PHILOSOPHY OF THE INDIAN CONSTITUTION	6				
Preamble, Salient Features						
UNIT - III	CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES	6				
Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.						
UNIT - IV	ORGANS OF GOVERNANCE	6				
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.						
UNIT - V	LOCAL ADMINISTRATION	6				
Municipalities: Introduction, Mayor and role of District's Administration head: Role and Importance, Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: ZilaPachayat. Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.						
TOTAL: 30 PERIODS						


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COURSE OUTCOMES:

Upon completion of the course, the students will be able to:

Course Outcome	Description	Bloom's Taxonomy Level
CO1	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.	Understand
CO2	Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.	Understand
CO3	Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.	Understand
CO4	Discuss the passage of the Hindu Code Bill of 1956.	Understand

REFERENCES:

1	The Constitution of India,1950(Bare Act),Government Publication.
2	Dr.S.N.Busi, Dr.B.R.Ambedkarframing of Indian Constitution, 1stEdition, 2015.
3	M.P. Jain, Indian Constitution Law, 7thEdn., Lexis Nexis,2014.
4	D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.


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23AC1134

நற்றமிழ் இலக்கியம்

L T P C
2 0 0 0

UNIT I

சங்க இலக்கியம்

6

1. தமிழின் துவக்க நூல் தொல்காப்பியம்
- எழுத்து, சொல், பொருள்
2. அகநானூறு (82)
- இயற்கை இன்னிசை அரங்கம்
3. குறிஞ்சிப் பாட்டின் மலர்க்காட்சி
4. புறநானூறு (95,195)
- போரை நிறுத்திய ஔவையார்

UNIT II

அறநெறித் தமிழ்

6

1. அறநெறி வகுத்த திருவள்ளுவர்
- அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புரவறிதல், ஈகை, புகழ்
2. பிற அறநூல்கள் - இலக்கிய மருந்து
- ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்)

UNIT III

இரட்டைக் காப்பியங்கள்

6


1. கண்ணகியின் புரட்சி
- சிலப்பதிகார வழக்குரை காதை
சமூகசேவை இலக்கியம் மணிமேகலை
- சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை

UNIT IV

அருள்நெறித் தமிழ்

6

1. சிறுபாணாற்றுப்படை
- பாரி முல்லைக்குத் தேர் கொடுத்தது, பேகன் மயிலுக்குத் போர்வை கொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள்
2. நற்றிணை
- அன்னைக்குரிய புன்னை சிறப்பு
3. திருமந்திரம் (617, 618)
- இயமம் நியமம் விதிகள்
4. தர்மச்சாலையை நிறுவிய வள்ளலார்
5. புறநானூறு
- சிறுவனே வள்ளலானான்


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6. அகநானூறு (4) - வண்டு
 நற்றிணை (11) - நண்டு
 கலித்தொகை (11) - யானை, புறா
 ஐந்திணை 50 (27) - மான்
 ஆகியவை பற்றிய செய்திகள்

UNIT V

நவீன தமிழ் இலக்கியம்

6

1. உரைநடைத் தமிழ்,
 - தமிழின் முதல் புதினம்,
 - தமிழின் முதல் சிறுகதை,
 - கட்டுரை இலக்கியம்,
 - பயண இலக்கியம்,
 - நாடகம்,
2. நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும்,
3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும்,
4. பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ் இலக்கியமும்,
5. அறிவியல் தமிழ்,
6. இணையத்தில் தமிழ்,
7. சுற்றுச்சூழல் மேம்பாட்டில் தமிழ் இலக்கியம்.

TOTAL: 30 PERIODS

தமிழ் இலக்கிய வெளியீடுகள் / புத்தகங்கள்

1. தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University) - www.tamilvu.org
2. தமிழ் விக்கிப்பீடியா (Tamil Wikipedia) - <https://ta.wikipedia.org>
3. தர்மபுர ஆதீன வெளியீடு
4. வாழ்வியல் களஞ்சியம் - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்
5. தமிழ்கலைக் களஞ்சியம் - தமிழ் வளர்ச்சித் துறை (thamilvalarchithurai.com)
6. அறிவியல் களஞ்சியம் - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்


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